Claim Amendments

Please amend claims 1-8, 10, and 12-17.

Please cancel claims 9, and 18-20.

Please add new claims 21-24 as follows:

Claims as Amended

1. (currently amended) A method for improving a photolithographic patterning process in a dual damascene process comprising the steps of:

providing ~~at least one~~ a via opening extending through a thickness of layers ~~sequentially~~ ~~including~~ comprising a dielectric anti-reflectance layer (DARC), ~~a hard mask layer~~, and ~~an~~ dielectric insulating layer ~~said via opening in closed communication with a conductive region underlying the insulating layer~~;

forming a resinous layer over the DARC layer to include filling the ~~at least one~~ via opening;

removing the resinous layer ~~overlying the at least one via opening~~ to expose the DARC layer to form ~~at least one~~ a via plug covering at least the dielectric insulating layer portion of the via sidewalls;

forming a photoresist layer over the DARC layer for photolithographically patterning a trench line opening disposed substantially over the ~~at least one~~ via opening;

photolithographically forming a trench line opening disposed substantially over the ~~at least one~~ via opening to expose a portion of the DARC layer forming a trench line pattern;

~~anisotropically~~ etching according to the trench line pattern through at least a thickness of the DARC layer ~~and hard mask layer~~ to include a portion of the ~~at least one~~ via plug; and,

~~anisotropically~~ etching according to the trench line pattern through a ~~portion of a~~ thickness portion of the dielectric insulating layer to form a trench line opening disposed substantially over a remaining portion of the ~~at least one~~ via opening.

2. (currently amended) The method of claim 1, wherein the dielectric insulating layer has a dielectric constant of less than about 3.0.

3. (currently amended) The method of claim 2, wherein the dielectric insulating layer comprises an interconnecting porous material.

4. (currently amended) The method of claim 2, wherein the dielectric insulating layer comprises carbon doped oxide.

5. (currently amended) The method of claim 1, wherein the ~~hard mask layer and~~ DARC layer comprises a metal nitride.

6. (currently amended) The method of claim ~~3~~ 1, wherein the ~~metal nitride~~ DARC layer is selected from the group consisting of ~~silicon nitride,~~ silicon oxynitride and titanium nitride.

7. (currently amended) The method of claim ~~4~~ 5, wherein the metal nitride is deposited according to a chemical vapor deposition process.

8. (currently amended) The method of claim 1, wherein the resinous layer comprises a photoresist resin ~~flowable at room temperature~~.

9. cancelled

10. (currently amended) The method of claim 1, wherein the step of ~~anisotropically~~ etching through a thickness of the DARC layer and hard mask layer to include a portion of the via plug ~~further~~ comprises reactive ion etching (RIE) with a nitrogen and oxygen containing plasma having a nitrogen to oxygen ratio of at least about 5.

11. The method of claim 9, said plasma further including hydrogen.

12. (currently amended) The method of claim 1, further comprising an ashing and cleaning process to remove the via plug following the step of ~~anisotropically~~ etching through the insulating layer to form a trench line.

13. (currently amended) A method for preventing the occurrence of undeveloped photoresist in semiconductor manufacturing process comprising the steps of:

providing ~~an anisotropically etched~~ first opening extending through a thickness ~~of layers sequentially including at least one~~ comprising an uppermost DARC metal nitride layer and ~~an~~ dielectric insulating layer;

forming an ~~resinous~~ I-line photoresist layer over the ~~at least one~~ DARC metal nitride layer to include filling the first opening;

removing the ~~resinous~~ I-line photoresist layer ~~overlying the etched opening~~ to expose the DARC metal nitride layer to form a plug filling the first opening at least up to an upper level of the dielectric insulating layer;

forming a DUV photoresist layer over the at least one metal nitride layer for lithographically patterning a second opening disposed over the first opening;

lithographically patterning a second opening disposed over the first opening to expose a portion of the ~~at least one~~ DARC metal nitride layer forming an etching pattern;

~~anisotropically~~ etching according to the etching pattern through at least a thickness of the ~~at least one~~ DARC metal nitride layer to include at least a portion of the plug; and,

~~anisotropically~~ etching according to the etching pattern through a thickness portion the dielectric insulating layer to form the second opening and a remaining portion of the first opening said second opening disposed substantially over the remaining portion of the first opening.

14. (currently amended) The method of claim 13, wherein the dielectric insulating layer has a dielectric constant of less than about 3.0.

15. (currently amended) The method of claim 14, wherein the dielectric insulating layer comprises ~~an~~ porous material including interconnecting pores.

16. (currently amended) The method of claim 14, wherein the dielectric insulating layer comprises carbon doped oxide.

17. (currently amended) The method of claim 13, wherein the ~~at least one~~ DARC metal nitride ~~includes at least one of~~ is selected from the group consisting of ~~silicon nitride,~~ silicon oxynitride and titanium nitride.

18. cancelled

19. cancelled

20. cancelled

21. (new) The method of claim 1, wherein the resinous layer is selected from the group consisting of an I-line photoresist, and a Novolac resin.

22. (new) The method of claim 1, wherein the thickness of layers further comprises a metal nitride hardmask layer underlying the DARC layer.

23. (new) The method of claim 1, wherein the step of removing the resinous layer comprises an RIE etchback process.

24. (new) The method of claim 23, wherein the etchback process is carried out to endpoint detection of the DARC layer.